



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

Certified that Sri/Smt. Sandipan Das from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on "Microelectronics Technology and VLSI Design" offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from 1st June 2023 to 6th July 2023. He/she has secured 'A+' grade in this course.

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Sourja Saha** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee

Co-ordinator

IC Design & Fabrication Centre

Electronics & Telecommunication Engg. Dept.

Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas

Head, Department of Electronics &

Telecommunication Engineering

Jadavpur University

Kolkata – 700032

Thursday, August 10, 2023



École de technologie supérieure
Département de génie électrique
1100, rue Notre Dame Ouest
Montréal (Québec) Canada H3C 1K3
Téléphone : 514 396 8829

SUBJECT: Letter of invitation for collaboration

Dear Dr. Raja Karmakar

It is my pleasure to initiate joint collaborative research between the Department of Computer Science and Engineering, Heritage Institute of Technology, Kolkata, India, and my team. Our focus lies in the broad domain of the implementation of artificial intelligence techniques in beyond 5G networks. In this context, we invite a team from your department to join us as researchers for one year, starting September 1, 2023. The collaboration can be initiated remotely, allowing your team to work from India. This collaboration is voluntary in nature.

I am looking forward to working with you.

Sincerely,

A handwritten signature in blue ink, appearing to read 'G. Kaddoum', is written over a horizontal line.

Professor Georges Kaddoum
Department of Electrical Engineering
École de Technologie Supérieure
1100, rue Notre-Dame Ouest Montréal (Québec) H3C 1K3 Canada
Email: georges.kaddoum@etsmtl.ca
Phone: 514 396-8923, Fax: 514 396-8684

NJIT

New Jersey Institute
of Technology

Heritage Institute of Technology Summer Research Program

Certificate of Completion

Awarded to

Arin Ghose



*For Successfully Completing a Six-Week
Independent Research Program at NJIT*

Summer 2023

July 28, 2023

*Atam Dhawan,
Interim Provost and Senior Executive Vice President*

*Durgamadhab Misra,
Program Director*

NJIT

New Jersey Institute
of Technology

Heritage Institute of Technology Summer Research Program

Certificate of Completion

Awarded to

Subhodeep Ghosh



*For Successfully Completing a Six-Week
Independent Research Program at NJIT*

Summer 2023

July 28, 2023

*Atam Dhawan,
Interim Provost and Senior Executive Vice President*

*Durgamadhab Misra,
Program Director*

NJIT

New Jersey Institute
of Technology

Heritage Institute of Technology Summer Research Program

Certificate of Completion

Awarded to

Poulami Basu



*For Successfully Completing a Six-Week
Independent Research Program at NJIT*

Summer 2023

July 28, 2023



*Atam Dhawan,
Interim Provost and Senior Executive Vice President*



*Durgamadhab Misra,
Program Director*

**1. Cover page: On Socio-Economic Growth, Inequity and Penetration Aspects
of the Information Technology Sector In India**

Submitted by: Arindam Chatterjee

Supervisor: Dr. Rimu Chaudhuri,
Associate Professor,
Heritage Business School, Kolkata

2. Details of RAC members present-

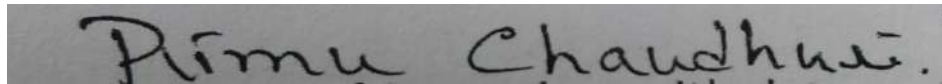
Dr Rimu Chaudhuri(Supervisor, Convener)

Designation..... Associate Professor

Tel033 6627 0600 / 0609/0614/0622/0623 *533 Mobile: 90512 55884

Email ID... rimu.chaudhuri@hbs.edu.in

Signature:

A rectangular box containing a handwritten signature in black ink that reads "Rimu Chaudhuri".

Date: 28th February, 2023



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Avishek Banerjee** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee

Co-ordinator

IC Design & Fabrication Centre

Electronics & Telecommunication Engg. Dept.

Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas

Head, Department of Electronics &

Telecommunication Engineering

Jadavpur University

Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Nayan Barua** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A+'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Ayan Saha** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Aratrika Bhattacharya** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on "**Microelectronics Technology and VLSI Design**" offered by IC Design & Fabrication Centre, Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured '**A+**' grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Shubhangi Nandy** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on "**Microelectronics Technology and VLSI Design**" offered by IC Design & Fabrication Centre, Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured '**A**' grade in this course.*

Sayan Chatterjee
Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas
Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Ayan Saha** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by

IC DESIGN & FABRICATION CENTRE

Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Anindya Chatterjee** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee
Prof. Sayan Chatterjee

Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas
Prof. Manotosh Biswas

Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Saikat Mitra** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on "**Microelectronics Technology and VLSI Design**" offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured '**A+**' grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Shaila Fiona Daniels** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by
IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

Certified that Sri/Smt. Mithun Mistri from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on "Microelectronics Technology and VLSI Design" offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from 1st June 2023 to 6th July 2023. He/she has secured 'A' grade in this course.

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032



Short Term Certified Summer Internship,
Training and Mentorship on



"MICROELECTRONICS TECHNOLOGY AND VLSI DESIGN"

Offered by

IC DESIGN & FABRICATION CENTRE
Electronics & Telecommunication Engineering Department,
Jadavpur University

*Certified that Sri/Smt. **Aryan Basu** from Heritage Institute of Technology, Kolkata. Successfully completed the Short Term Certified Summer Internship Training and Mentorship on **"Microelectronics Technology and VLSI Design"** offered by IC Design & Fabrication Centre, Electronics & Tele-communication Engineering Department, Jadavpur University, Kolkata in collaboration with Electronics Centre of Excellence, Bhubaneswar from **1st June 2023 to 6th July 2023**. He/she has secured **'A'** grade in this course.*

Sayan Chatterjee

Prof. Sayan Chatterjee
Co-ordinator
IC Design & Fabrication Centre
Electronics & Telecommunication Engg. Dept.
Jadavpur University, Kolkata – 700032

Manotosh Biswas

Prof. Manotosh Biswas
Head, Department of Electronics &
Telecommunication Engineering
Jadavpur University
Kolkata – 700032

Portion of Internship Offer Letter by DXCorr
to Students is Shown



Date: **05-04-2023**

Dear Ankit Kumar,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Md. Anwar Raza,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Aindrila Chowdhury,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 16,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: 05-04-2023

Dear Pritam Samanta,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Niraj Kumar ,

Sub: Letter of Internship Offer

We welcome you to DXCorr Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCorr Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Shreyashee Roy,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Supritey Dey,

Sub: Letter of Internship Offer

We welcome you to DXCorr Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCorr Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Soumya Biswas,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: 05-04-2023

Dear Suman Satick,

Sub: Letter of Internship Offer

We welcome you to DXCorr Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCorr Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Shubhashree Das,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 16,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Vinayak Gupta,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: **05-04-2023**

Dear Upasana Roy,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**

You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.



Date: 05-04-2023

Dear Susnata Banerjee,

Sub: Letter of Internship Offer

We welcome you to DXCORR Hardware Technologies and congratulate you on being appointed as **Intern -VLSI Engineer.**



You will be entitled to receive a monthly compensation of 14,333 INR for the duration of your internship with DXCORR Hardware Technologies.

Please scan and enclose the mentioned docs for our records.

1. One (1) recent color passport size photograph.
2. A legible copy of your Aadhar card.
3. A legible copy of your PAN card.

Find a journal

Publish with us

 Search Cart[Home](#) > [Innovations in Systems and Software](#)

S.I. : Coupling Data and Software Engineering to

Power-aware partitioning 3D-SoC

[Sabyasachee Banerjee](#) , [Subhashis Majumder](#), [Bhargab B. Bhattacharya](#) & [Debesh K. Das](#)[Innovations in Systems and Software Engineering](#) (2022) | [Cite this article](#)51 Accesses | [Metrics](#)

Abstract


The technology of 3D-ICs has been widely used in designing core-based systems-on-chip (SoC), which comprises vertical stacking of multiple silicon and metal layers, interconnected using through-silicon vias (TSV). Testing of the embedded cores in such a device not only

Bhargab B. Bhattacharya

Department of Computer Science and Engineering, Indian Institute of Technology
Kharagpur, Kharagpur, WB, 721302, India

[View author publications](#)

You can also search for this author in
[PubMed](#) | [Google Scholar](#)

[institution](#) 

on:

[Computer Science](#) [SDG 7: Affordable and Clean Energy](#)

Access options

[Buy article PDF](#)

39,95 €

Price includes VAT (India)

Journal Pre-proofs

A Decision Framework with Nonlinear Preferences and Unknown Weight Information for Cloud Vendor Selection

Mohuya Byabartta Kar, Raghunathan Krishankumar, Dragan Pamucar, Samarjit Kar

PII: S0957-4174(22)02000-0
DOI: <https://doi.org/10.1016/j.eswa.2022.118982>
Reference: ESWA 118982

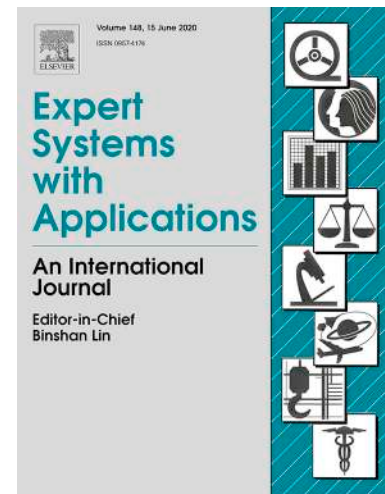
To appear in: *Expert Systems with Applications*

Received Date: 22 March 2022
Revised Date: 29 September 2022
Accepted Date: 3 October 2022

Please cite this article as: Byabartta Kar, M., Krishankumar, R., Pamucar, D., Kar, S., A Decision Framework with Nonlinear Preferences and Unknown Weight Information for Cloud Vendor Selection, *Expert Systems with Applications* (2022), doi: <https://doi.org/10.1016/j.eswa.2022.118982>

This is a PDF file of an article that has undergone enhancements after acceptance, such as the addition of a cover page and metadata, and formatting for readability, but it is not yet the definitive version of record. This version will undergo additional copyediting, typesetting and review before it is published in its final form, but we are providing this version to give early visibility of the article. Please note that, during the production process, errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

© 2022 Elsevier Ltd. All rights reserved.



On Density of Grid Points in l_∞ -Balls

Nilanjana G. Basu¹[0000-0001-5053-7517], Partha Bhowmick²[0000-0003-2765-7777], and Subhashis Majumder¹[0000-0002-0849-9016]

¹
Department of Computer Science and Engineering, Heritage
Institute of Technology, Kolkata, India
{nilanjanag.basu,subhashis.majumder}@heritageit.edu <https://www.heritageit.edu/CSE.aspx>

²
Department of Computer Science and Engineering,
Indian Institute of Technology, Kharagpur, India pb@cse.iitkgp.ac.in
<https://cse.iitkgp.ac.in/~b/>

Abstract. Finding the minimum and the maximum densities for axes-parallel squares, cubes, and hypercubes, cast in the integer space, is an important problem in the domain of digital geometry. In this work, we study different variations of this problem and solve a number of them. Interestingly, the extremum values for integer sizes sometimes differ from those for real sizes, and hence, we have studied and analyzed them separately. Further, the results and proofs in 2D readily extend to higher dimensions, and hence we could get simple-yet-novel theoretical results for the extremum densities for l_∞ -balls in general. As ‘density’ provides a measure of how a set of points bounded by a region is relatively more concentrated or sparse, it has applications in image analysis, social networking, complex networks and related areas, apart from different branches of physical science. Hence, our results are fundamental in the understanding of locating the density minima and maxima in a discrete space of an arbitrarily large dimension.

Keywords: Digital square • Digital Cube • Digital Hypercube • Digital geometry • Pixel density • Geometry of numbers

1 Introduction

In the domain of discrete and computational geometry, acquiring the knowledge of a particular fact is of paramount importance – how dense or how clustered a specific set of points is, compared to a given set within a given shape or region. It has been easily noticed in the domain of Social Networking and Complex Networks which got established as some of the mostly popular areas recently.

1.1 Existing work

In 2D, ‘Density of points’ of an unweighted set of points is expressed as the number of points per unit area [11]. In case of a weighted set of points, it is the sum of the weights divided by the area of that region. Later Basu et al. [3] proposed algorithms for finding maximum- and minimum-density regions for higher dimensions. In the domain of digital geometry, quite a handful of work [7,10,12, 13] has been done related to digital discs and digital balls defined on square or non-square grid.