

HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE

<ECE>

M. Tech 1st Year 2nd Semester

VLSI

SESSION: 2024-2025

DAY	GROUP	9.00 AM – 10.00 AM	10.00 AM – 11.00 AM	11.00 AM – 12 NOON	12 NOON – 1.00 PM	1.00 PM – 2.00 PM	2.00 PM – 3.00 PM	3.00 PM – 4.00 PM	4.00 PM – 5.00 PM	5.00 PM – 6.00 PM
MON	GR. 1	L/VLSI 5202 /OB/ICT 614	L/VLSI 5232 /KD/ICT 614	L/VLSI 5241/AS/ICT 614	BREAK	LAB/VLSI 5251/KM/ AR*/ICT 602				
	GR. 2									
TUE	GR. 1	L/VLSI 5241/AS/ICT 614	L/VLSI 5201/KM/ICT 614	BREAK		L/VLSI 5202 /OB/ICT 614	VLSI 5293/DM/ ICT 614			
	GR. 2									
WED	GR. 1	L/VLSI 5242/AK/ICT 614	L/VLSI 5202 /OB/ICT 614	L/VLSI 5232 /KD/ICT 614	BREAK	L/VLSI 5201/KM/ICT 614	VLSI 5293/KM/ ICT 614			
	GR. 2									
THU	GR. 1	LAB/VLSI 5252/AMB/ PS*/ICT602				L/VLSI 5232 /KD/ICT 614	BREAK	MENTORING		
	GR. 2									
FRI	GR. 1	L/VLSI 5201/KM/ ICT 614	L/VLSI 5242/AK/ ICT 614	L/VLSI 5241/AS/ICT 614	BREAK	REMEDIAL ICT 614				
	GR. 2									

To be Effective from 19 .02.2025

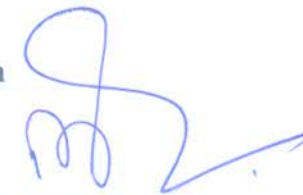
A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination
Students should target 100% attendance



Member



HOD



Principal

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COURSE STRUCTURE:

A. Theory							
Sl. No.	Course Code	Course Name	Contact Hours/Week				Credit Points
			L	T	P	Total	
1	VLSI5201	VLSI Processor Architecture	4	0	0	4	4
2	VLSI5202	VLSI Design, Verification and Testing	4	0	0	4	4
3	VLSI5203	Analog IC Design	4	0	0	4	4
4		Elective - II					
	VLSI5231	Advanced Micro & Nano Devices	4	0	0	4	4
	VLSI5232	DSP Algorithms for VLSI System Design					
5		Elective - III					
	VLSI5241	Low Power VLSI Circuit and System	4	0	0	4	4
	VLSI5242	Sensors					
Total Theory						20	20
B. Practical							
6	VLSI5213	Analog VLSI Design Laboratory	0	0	3	3	2
Total of practical						3	2
C. Sessional							
7	VLSI5221	Term paper leading to thesis	0	4	0	4	3
Total Sessional						4	3
Total of Semester						27	25


L/VLSI
5201/KM/
ICT 614

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