Memorandum of Understanding

Between

Electronics Center of Excellence (e-COE)

And

Heritage Institute of Technology,

Kolkata

Memorandum of Understanding

About Electronics Center of Excellence (e-COE):

e-COE (Electronics Center of Excellence) has been established by Electronics Sector Skills Council of India (**ESSCI**), GOI, **under the Skill India program of Govt. of India** under mentorship of India Electronics & Semiconductor Association (**IESA**). The center is located at DCB-621, DLF Cyber City, Patia, Bhubaneswar.

Electronic Center of Excellence (**e-COE**) is a localized hub with three primary focus areas –

1) Industry oriented Training for Electronics System Design & Manufacturing (ESDM)
2) Industry-Academia Research for productization
3) Incubations with Technology solutions for social impact

As one of the primary responsibility, **e-COE** provides industry oriented semiconductor electronics courses in VLSI Domain. Pedagogy of these courses are based on direct guidance of **ESDM** Industry experts. Each training program also have a counselling, interaction and mock interview by **ESDM** industry experts and industry partners.

At the end of the course the students are certified by **e-COE**. In addition to this, **ESSCI** conducts an assessment test based on which ESSCI certification is provided to qualified students. So by the end of course, students get a Govt. of India certification in VLSI training. e-COE provides Placement Assistance to the trained students, e-COE helps students to get connected to Internship Opportunities at the end of the courses.

About Heritage Institute of Technology, Kolkata (HITK):

Heritage Institute of Technology, 994, Madurdaha, Chowbaga Road, Anandapur, P.O. East Kolkata Township, Kolkata – 700107, West Bengal, India, is a **NBA, NAAC** accredited **leading Private Engineering college** as established in 2001 and affiliated to Maulana Abul Kalam Azad University of Technology, West Bengal (formerly known as West Bengal University of Technology). This institute gained **'Autonomous Status'** in 2014. Heritage Institute of Technology is a leading College offering (a) Undergraduate and Postgraduate courses in (i) Engineering and Technology and (ii) Applied Sciences, leading to **B.Tech, M.Tech and MCA Degrees** in different disciplines.

Electronics Center of Excellence (**e-COE**) hereinafter will be called and referred to as "**e-COE**" (which term of expression shall, unless excluded by or repugnant to the context or subject, be deemed to mean and include its successors-in-office, administrators, legal representatives and/or assigns) on the ONE PART

and

Heritage Institute of Technology, Kolkata (**HITK**) hereinafter will be called and referred to as "**HITK**" (which term of expression shall, unless excluded by or repugnant to the context or subject, be deemed to mean and include its successors-in-office, administrators, legal representatives and/or assigns) on the OTHER PART.

1. Purpose of the Agreement:

e-COE and **HITK** have mutually agreed to work together for:

1) Industry oriented **Training** for Electronics System Design & Manufacturing (**ESDM**)
2) Industry-Academia **Research** for productization

e-COE and **HITK** have mutually agreed to work together for training of **HITK** students on VLSI and its related domain at the **e-COE** Center to make them employable in core Semiconductor Industry. **e-COE** also works closely with its industry partner in semiconductor area and gets them connected to the students for possible scope of **internship** and **job** in respective organizations.

Another priority is to endeavor into state-of-the-art collaborative **Research** in the field of Electronic System Design and Manufacturing (**ESDM**) and Internet of Things (**IoT**).

e-COE and **HITK** envision this partnership to excel the growth of **ESDM** manpower development and research mindset in Electronics promoting the initiative of **Make-in-India**. This agreement describes their understandings and commitments to this effort.

2. Scope and Duration:

e-COE and **HITK** will work together to bring & train the students into the domain of VLSI for various employment oriented programs. They will also engage into collaborative Research in VLSI Domain.

Initial duration of this agreement is from **September 25, 2018** to **September 24, 2020**. The same can be renewed in future on mutually agreed terms & conditions.

The aforementioned agreement shall specifically be focused and will execute in the following way:

Partnership related to Training –

i. **HITK** will encourage their students to join for different Industrial training programs of **e-COE** depending upon the course levels and the batch of the student. For example, if the students who have passed second year may join in basic VLSI Design Engineer Course, whereas those who have completed the VLSI Design Engineer Course can join Cadence based Physical Design/Analog Design Engineer & other higher-level courses etc.

ii. There are Industrial Training programs to be completed by students as per **HITK** Autonomy Syllabus as well as Curriculum prescribed by AICTE. Students successfully completing **e-COE** Industrial training programs will achieve full credits.

iii. The students will get a completion certificate after the end of course from **e-COE**. Then **e-COE** will arrange for **ESSCI** (Electronics Sector Skills Council of India) certification examination after the end of the course. **e-COE** will ensure no clash of examinations of **e-COE** with that of **HITK**.

iv. At the end of **e-COE** certification, students are highly encouraged to continue a project in the domain in **HITK** VLSI LAB. Some level of guidance / assistance will be provided by **e-COE** Experts through occasional review till passing out of the program, at no extra cost.

v. 40 students can be trained in a batch at a given time.

vi. Students will be exposed to semiconductor industry bodies increasing the potential of internship opportunities and/or direct placement in core sector companies for Electronics.

vii. Overall training offerings are distributed in three levels of program- Level 1, Level 2 and Level 3. Level 1 is a basic program with general exposure to various aspects of the domain. Level 2 goes to specific of a particular vertical e.g. Digital Design or Analog design. Level 3 is on hands on project for a specific niche skill e.g. Analog layout or Physical design.

viii. Students based on their ability and interest can start from level 1 and move up the value chain. Interested industry partners will also start interacting post level 1 training is completed.

ix. Interested Students who will join the Training Programs need prior permission of Institute authority and will bear Training Cost depending on course Level. **e-COE** VLSI Training Program is shown below.

Electronic Center of Excellence (e-COE) VLSI Training Program

Name of Program	Duration	Key Contents	Purpose	Eligibility
Level 1: VLSI Design Engineer	4 weeks (250 hrs)	Basics of Digital and Analog design, Simple CMOS IC Design and layout	Entry level training providing a hands-on exposure of different domains in ESDM.	2nd / 3rd Year B Tech 1st Year M Tech
Level 2: Analog Design Engineer	6 weeks (300 hrs)	Analog/Mixed Signal Design and Layout, CMOS circuit design basics	Beginners training into Analog design basics with hands-on experience.	Completion of Level1 3rd/4th Year B Tech 2nd Year M Tech
Level 2: Digital Design Engineering	6 weeks (300 hrs)	Fundamentals of Digital Circuits and Systems, CMOS Digital Circuits and Analysis	Beginners training into Digital front end and back end design with hands on experience.	Completion of Level1 3rd/4th Year B Tech 2nd Year M Tech
Level 3: Internship	6 months-1 year	Chip design project on Analog, Digital Design or hardware characterization	Live project execution on projects relevant to industry	Completion of L1 and L2 (any one) Final year B Tech Final Year M Tech

Partnership related to Research –

i. **e-COE** is engaged in development of Integrated chips of VLSI designs for advance **IoT** applications. **HITK** faculty and students will be allowed to participate in this research program and be part of Chip development in latest Technologies.

ii. One of the Research and Development (R & D) plan is collaborative Micro-chip development where **HITK** team with own embedded Memory Design for Venus Chip (**India Chip Program**) to be fabricated in **TSMC** (Taiwan Semiconductor Manufacturing Corporation) in 65nm Process, one of the latest Technology.

iii. For collaborative research, special preference will be given to students who already completes the necessary training with **e-COE**.

iv. The VLSI chip design can be shown as final year B.Tech project during 4th year and/or final year M Tech VLSI project. Necessary access to Technology and CAD Tools (Software and Hardware) will be provided at **e-COE** center and **HITK** VLSI LAB as needed.

v. On successful completion of the Research, design will be reviewed by industry experts and will be part of Silicon Fabrication.

vi. It is expected and assumed that several papers and patents can be developed out of this exercise.

3. **Decision-making structure & authority:**

e-COE and HITK each will identify one person (SPOC) within their own organization to serve and execute the program smoothly.

4. **Legal & financial structure:**

The **e-COE** will be responsible for the completion of the training. In case not completed, legally **e-COE** will return cost for training fully to concerned **HITK** Students.

5. **Resource Commitment to the Collaboration:**

e-COE will make sure that best of the faculty members are taking classes for the training of the **HITK** students.

6. **Commercialization:**

The output from the training program/project can be published/shown as the joint collaboration work of **e-COE** and **HITK**.

7. **Termination of this agreement:**

HITK or **e-COE** retains the right to withdraw from the collaboration upon giving the other participating organizations at least 30 days prior notice of its decision to withdraw.

8. **Extension or Amendment of this agreement:**

This agreement may be extended or amended only through unanimous agreement between **e-COE and HITK**. The decision to amend or extend the agreement, and language describing the agreed upon changes, shall be documented in writing, including the date of the amendment/extension, and the signatures of the Director/Concerned Authority of each participating organization.

9. **Disputes and differences of this agreement:**

Both **e-COE** and **HITK** agree that disputes and differences, if any, arising out of this Memorandum regarding interpretation of any of the terms and conditions herein contained or touching these presents or determination of any liability, residual or otherwise, shall be resolved, reconciled and settled amicably through dialogue and discussion between the parties. If needed a committee can be formed involving members of **e-COE** and **HITK** management.

This agreement was unanimously adopted by designated representatives of **e-COE** and **HITK** on date: 03/10/**-2018**.

Principal
HITK

Principal
Heritage Institute of Technology

Heritage Institute of Technology ★ Kolkata ★

Date: 3. 10. 2018

Director
e-COE

Date: 3-10-2018

Electronics Center of Excellence ★ DCB-621, DLF Cyber City, Patia, BBSR ★ e-COE